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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,536	11/13/2003	Ralf Brederlow	V0195.0003	2199

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EXAMINER	
RODGERS, COLLEEN E	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary	Application No.	Applicant(s)	
	10/714,536	BREDERLOW, RALF	
	Examiner	Art Unit	
	Colleen E. Rodgers	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Amendment filed 9 April 2006. By this amendment, claims 13 and 24 are amended. Claims 13-24 remain pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13-17 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bao et al** (USPN 6,150,668).

Regarding claims 13 and 24, **Bao et al** discloses a polymer transistor arrangement and a method of forming said arrangement, comprising:

forming a polymer transistor in and/or on a substrate **205** including:

forming a first source/drain region **225**;

forming a second source/drain region **226**;

forming a channel region **230** between the first and second source/drain regions **225** and **226**;

forming a gate region **215**; and

forming a gate insulating layer **220** between the channel region **230** and the gate region **215**; and

forming a drive circuit [see col. 9, lines 33-34].

Bao et al does not specifically mention providing voltages such that the polymer transistor has properties similar or identical to those of a Schottky diode. However, this is merely an intended use of the structure as taught by **Bao et al**. It has been held that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). It would have been obvious to one of ordinary skill in the art at the time of invention to apply external stimuli such as voltages in any manner as best befits the application for which the structure is intended.

Regarding claim 14, **Bao et al** disclose the arrangement of claim 13 as described above. That the drive circuit provides the source/drain region and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-bias diode is merely an intended use, and therefore anticipated by **Bao et al** as the structure of **Bao et al** may be used in this manner.

Regarding claim 15, **Bao et al** disclose the arrangement of claim 13 as described above, wherein the channel region **230** and the source/drain regions **225** and **226** are produced from a material such that the junction between one of the source/drain regions **225** or **226** and the channel region **230** is a Schottky junction [see paragraph bridging cols. 6 and 7]. It is admitted in the instant specification that:

> A Schottky diode is a diode which, instead of a pn junction, uses a metal-semiconductor contact or a metal-polymer contact, the metal having a different work function that the other material that it is contact connected [see instant specification, page 4, lines 4-6].

Therefore, the structure of **Bao et al** must function in the same way.

Regarding claim 16, **Bao et al** disclose the arrangement of claim 13 as described above. As with claim 17, that the drive circuit provides electrical potentials such that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions is merely an intended use, and therefore anticipated by **Bao et al** as the structure of **Bao et al** may be used in this manner.

Regarding claim 17, **Bao et al** disclose the arrangement of claim 13 as described above, wherein the junctions between respective ones of the source/drain regions **225** and **226** are formed geometrically asymmetrically with respect to one another [see Figs. 2 and 3].

Regarding claims 19-23, **Bao et al** disclose the arrangement of claim 13 as described above. The limitations of claims 19-23 are merely intended use, and therefore are anticipated by **Bao et al** as the structure of **Bao et al** as disclosed may be used in an integrated circuit device, as a reference voltage circuit, a temperature-compensated reference voltage circuit, a current source or a voltage control circuit.

4. Claims 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Jackson et al** (USPN 6,720,572).

Regarding claims 13 and 24, **Jackson et al** disclose a polymer transistor arrangement and a method of forming said arrangement, comprising:

a polymer transistor formed in and/or on a substrate **10** including:

forming a first source/drain region **18**;

forming a second source/drain region **24**;

forming a channel region **20, 22** between the first and second source/drain regions **18** and **24**;

forming a gate region **14**; and

forming a gate insulating layer **16** between the channel region **20, 22** and the gate region **14**; and

forming a drive circuit [see Fig. 2; see also col. 3, lines 45-48].

Jackson et al does not specifically mention providing voltages such that the polymer transistor has properties similar or identical to those of a Schottky diode. However, this is merely an intended use of the structure as taught by **Jackson et al**. It has been held that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). It would have been obvious to one of ordinary skill in the art at the time of invention to apply external stimuli such as voltages in any manner as best befits the application for which the structure is intended.

Regarding claim 14, **Jackson et al** disclose the arrangement of claim 13 as described above. That the drive circuit provides the source/drain region and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-bias diode is merely an intended use, and therefore anticipated by **Jackson et al** as the structure of **Jackson et al** may be used in this manner.

Regarding claim 15, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein the channel region **20, 22** and the source/drain regions **18** and **24** are produced from a material such that the junction between one of the source/drain regions **18** or **24** and the channel region **20, 22** is a Schottky junction. Specifically, the channel region is formed of a material such as

pentacene and 8-hydroxyquinoline aluminum (Alq) and the source/drain regions are formed from palladium and aluminum [see col. 3, lines 59-64]. It is admitted in the instant specification that:

> A Schottky diode is a diode which, instead of a pn junction, uses a metal-semiconductor contact or a metal-polymer contact, the metal having a different work function that the other material that it is contact connected [see instant specification, page 4, lines 4-6].

Therefore, the structure of **Jackson et al** must function in the same way.

Regarding claim 16, **Jackson et al** disclose the arrangement of claim 13 as described above. As with claim 17, that the drive circuit provides electrical potentials such that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions is merely an intended use, and therefore anticipated by **Jackson et al** as the structure of **Jackson et al** may be used in this manner.

Regarding claim 17, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein the junctions between the respective ones of the source/drain regions **18** and **24** and the channel region **20, 22** are formed geometrically asymmetrically with respect to one another [see Fig. 1].

Regarding claim 18, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein one of the source/drain regions **24** is formed at least partially on the channel region **20, 22** and the other source/drain region **18** is formed at least partially below the channel region **20, 22** [see Fig. 1].

Regarding claims 19-23, **Jackson et al** disclose the arrangement of claim 13 as described above. The limitations of claims 19-23 are merely intended use, and therefore are anticipated by **Jackson et al** as the structure of **Jackson et al** as disclosed may be used in an integrated circuit device, as a reference voltage circuit, a temperature-compensated reference voltage circuit, a current source or a voltage control circuit.

Response to Arguments

5. Applicant's arguments with respect to claims 13-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CER

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